

Synopsys Design Compiler Doentation

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Collaboration Brings Integrated and Validated IP, Design Tools and Methodology to Facilitate Low Power, High-performance Mobile System-on-Chip Design MOUNTAIN VIEW, Calif., Jan. 17, 2011-- Synopsys ..

Synopsys Announces Production-Ready Lynx Design System Optimized for Common Platform 28-nm High-K Metal Gate Technology
To achieve this, special consideration was given to the design hierarchy and documentation, as well as RTL coding ... The synthesis scripts provided with the CoolFlux DSP coreKits use Synopsys Power ...

Collaboration Makes New Commercial Ultra Low-Power Solution Accessible To Designers
You can read the documentation in the HACKING file for details on the architecture. Briefly, the instruction 's top four bits encode the operation, while the last four bits select the register ...

Teach Yourself Verilog With This Tiny CPU Design
Synopsys revealed a power analysis solution for early SoC design as well as signoff-accurate power and ... The kit includes tool qualification guidelines, tool documentation, quality assurance ...

The Week In Review: Design
" Debug is on the top of our customers mind all the time," says Swami Venkat, senior director of strategic programs in the verification group of Synopsys ... RTL design, test-bench components, ...

Debug: The Schedule Killer
Its new tool, the Wasga Compiler ... on Chip Design. " The book provides a hands-on, how-to guide for semiconductor design. Last on the list, but certainly not least, was Synopsys announcement ...

20 nm Chips, 3D ICs, Low Power and Fast Tools Are Themes Of DAC 2012
First, writing such a " compiler " is complicated. It involves intimate knowledge of the resources available on the FPGA that can assimilate the functionality of the intended design. Second ...

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