High Performance Asic Design Using Synthesizable Domino Logic In An Asic Flow

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An overview of design techniques used to achieve high speed in ASIC designs is followedbychaptersdescribingthedesignandcharacterizationofdominologicstandard cell libraries and an advanced domino logic synthesis ?ow. Actual results achieved by using automated domino logic design techniques, including silicon measurements, are presented to validate the methodology, whilst real-world design examples, such as the implementation of the execution unit of a microprocessor and Viterbi decoder ...

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High Performance Asynchronous ASIC Back-End Design Flow ...
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Although an initial investment is required to develop an ASIC, the payoff for this investment is very high. Aside from a possible performance enhancement, a product using an ASIC requires fewer electronic components and is much cheaper to assemble. Having fewer parts translates into higher reliability overall.

What is an ASIC, and why is everyone using them? - Sigenics
due to irM use), which almost is a synonym for hardware design, VLSI design, or ASIC synthesis. Technology-independent Performance Evaluation. Fig. 11 summarizes acceleration factors hav-

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cluding ASIC, FPGA, and SoC. Traditional NICs are ASIC-based, with predefined network semantics baked into hardware. While these offer the best price/performance, they are generally not programmable. Some vendors have shipped high-core-count, pro-grammable ASIC-based SmartNICs [23], but they are famously

SmartNIC Performance Isolation with FairNIC: Programmable ...
By the mid-1980s, the limitations of the ASIC were becoming apparent in the manufacturing process with many designers having to use specific tools to complete the design which drove up the costs. The creation of standard cells helped to improve gate density and provide for excellent performance while cutting down the cost of manufacturing the ASIC.

Understanding ASIC Development - AnySilicon
More than just a chip, the GRN1 features improvements to the hashing boards, control boards, mechanical design, and even the PSU. ... producers of high-performance ASIC miners for cryptocurrency.

The Obelisk GRN1: An ASIC for Grin | by David Vorick ...
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As FPGA design is merely an RTL code, this allows engineers to use a traditional ASIC design flow: Logic synthesis, floorplanning, synthesis

and layout. The following are the requires steps based on an article from AnySilicon.com . ASIC Design Flow Step 1: Logic Synthesis . RTL conversion into netlist; Design partitioning into physical blocks

Understanding FPGA to ASIC Conversion - HardwareBee
An application-specific integrated circuit (ASIC / ? e? s ? k /) is an integrated circuit (IC) chip customized for a particular use, rather than intended for general-purpose use. For example, a chip designed to run in a digital voice recorder or a high-efficiency bitcoin miner is an ASIC. Application-specific standard product (ASSP) chips are intermediate between ASICs and industry standard ...

Application-specific integrated circuit - Wikipedia
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