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total logical effort of a 2-inputNANDgate ” is the logical effort of both inputs taken together, while “ the logical effort of a 2-inputNAND gate ” is the logical effort per input of one of its two inputs. The logical effort of an input group is de fi ned analogously to the logical effort per input, shown in the previous section.

Chapter 4 Calculating the Logical Effort of Gates
Logical effort: designing fast CMOS circuits . 1999. Abstract. No abstract available. Cited By. Schneider E and Wunderlich H GPU-accelerated time simulation of systems with adaptive voltage and frequency scaling Proceedings of the 23rd Conference on Design, Automation and Test in Europe, (879-884)

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Logical Effort: Designing for Speed on the Back of an Envelope David Harris ... Table 1: Logical effort of static CMOS gates. Gate type Number of inputs 12345n inverter 1 NAND 4/3 5/3 6/3 7/3 (n+2)/3 NOR 5/3 7/3 9/3 11/3 (2n+1)/3 ... How fast can the decoder operate? 4:16 Decoder.

~~Logical Effort: Outline~~

The method of logical effort, a term coined by Ivan Sutherland and Bob Sproull in 1991, is a straightforward technique used to estimate delay in a CMOS circuit. Used properly, it can aid in selection of gates for a given function (including the number of stages necessary) and sizing gates to achieve the minimum delay possible for a circuit.

~~Logical effort - Wikipedia~~

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5: Logical Effort CMOS VLSI Design Slide 26 Designing Fast Circuits qDelay is smallest when each stage bears same effort qThus minimum delay of N stage path is qThis is a key result of logical effort – Find fastest possible delay – Doesn ' t require calculating gate sizes D= ∑ dDP iF =+ ^ 1 N f==g ii hF 1 D=+NFP N